CLAIMS

1. A method for generating expect digital signals for a series of applied digital signals having a known sequence to determine if applied digital signals are being properly captured, comprising:

capturing a first group of the applied digital signals;

generating a group of expect digital signals from the captured first group of applied digital signals;

capturing a second group of the applied digital signals after the first group; and

determining the second group of applied digital signals was properly captured when the second captured group of applied digital signals corresponds to the generated group of expect digital signals.

2. The method of claim 1 wherein the series of applied digital signals comprises a 15 bit pseudo-random bit sequence of digital signals.

3. The method of claim 2 wherein the 15 bit pseudo-random bit sequence comprises the repeating bit sequence of "111101011001000."

4. The method of claim 1 wherein each group comprises four data signals.

5. The method of claim 1 wherein each group of applied digital signals includes four digital signals, and generating the group of expect digital signals comprises:

storing the four digital signals of the first group on respective first through fourth output nodes;

developing a first logic signal from the signal on the four output nodes;

developing a second logic signal from three of the four signals on the four output nodes;

coupling either the digital signal on the first output node or the complement of this digital signal to a first storage node responsive to the first logic signal to develop a first expect digital signal on the first storage node;

coupling either the digital signal on the second output node or the complement of this digital signal to a second storage node responsive to the second logic signal to develop the second expect data signal on the second storage node;

coupling either the data signal on the third output node or the complement of this data signal to a third storage node responsive to the data signal on the first output node and the data signal on the fourth output node to develop the third expect data signal on the third storage node;

coupling either the data signal on the fourth output node or the complement of this data signal to a fourth storage node responsive to the data signal on the first output node to develop the fourth expect data signal on the fourth storage node; and

coupling the first through fourth storage nodes to the first through fourth output nodes, respectively, to apply the four expect data signals on these respective nodes.

6. A method for synchronizing a clock signal applied on a clock terminal of an SLDRAM, comprising:

placing the SLDRAM in a synchronization mode;

applying the clock signal;

generating an internal clock signal responsive to the external clock signal, the internal clock signal having a phase relative to the external clock signal;

applying a repeating sequence of digital signals on each of a plurality of data terminals of the SLDRAM, each sequence having a known pattern;

capturing a group of digital signals on each of the data terminals responsive to the internal clock signal;

generating a series of expect data groups, each expect data group including a plurality of expect digital signals having values determined in response to the values of expect digital signals in the preceding expect data group, and the values of the digital signals in the first expect data group being determined responsive to digital signals from one of the captured groups of digital signals;

capturing a subsequent group of digital signals applied on the data terminals responsive to the internal clock signal;

comparing the digital signals in the subsequent group to the expect digital signals in the corresponding expect data group, and determining the subsequent group was successfully captured when each of the digital signals the subsequent group has its expected value;

storing the results of this comparison;

adjusting the phase of the clock signal;

repeating the acts of capturing a subsequent group of digital signals through adjusting the phase of the internal clock signal until a predetermined number of phases have been utilized for the internal clock signal; and

selecting a phase of the internal clock signal from one of stored phases that successfully captured the applied digital signals.

7. The method of claim 6 wherein applying a repeating sequence of digital signals on each of a plurality of data terminals comprises applying a true repeating 15 bit pseudo-random bit sequence on every other data terminal and applying the complement of this true sequence on those data terminals not receiving the true sequence.

8. The method of claim 6 wherein each group comprises four digital signals.

9. The method of claim 6 wherein the digital signals from one of the captured groups of digital signals used to determine the digital signals in the first

expect data group comprise four captured digital signals applied sequentially on a FLAG terminal of the SLDRAM.

10. The method of claim 6 wherein comparing the digital signals comprises comparing the digital signals in a predetermined number of subsequent groups to their corresponding expect digital signals for each phase of the internal clock signal, and determining captures for a respective phase were successful only when the digital signals in all subsequent groups have their corresponding expected values.

11. A method for generating an expect data pattern from an applied bit stream having a known pattern, comprising capturing a first group of bits from the applied bit stream, and generating an expected group of bits having values determined by the values of the captured first group of bits.

12. The method of claim 11 wherein the applied bit stream comprises a 15-bit pseudo-random bit sequence.

13. The method of claim 12 wherein the 15 bit pseudo-random bit sequence comprises the repeating bit sequence of "111101011001000."

14. The method of claim 11 wherein the captured first group of bits includes 4 bits.

15. A method of adaptively adjusting the phase of an internal clock signal relative to an external clock signal, the internal clock signal triggering a latch to store a digital signal, the method comprising:

repetitively applying digital signals to the latch in a known repeating sequence;

storing a first group of digital signals in the latch responsive to the internal clock signal having a first phase;

generating expected values for a next group of digital signals to be stored in the latch responsive to the stored first group of digital signals;

storing a second group of digital signals in the latch responsive to the internal clock signal having the first phase;

comparing the digital signals of the second group to their expected values to determine if the stored digital signals were successfully captured by the latch, and storing the results of this comparison;

repeating the acts of repetitively applying digital signals to comparing the digital signals for a plurality of phases of the internal clock signal; and

selecting a phase of the clock signal that caused the latch to store digital signals having the expected values.

16. The method of claim 15 wherein repetitively applying digital signals comprises applying a repeating 15 bit pseudo-random bit sequence of digital signals.

17. The method of claim 16 wherein the 15 bit pseudo-random bit sequence comprises the repeating bit sequence of "111101011001000."

18. The method of claim 15 wherein each group comprises four digital signals.

19. The method of claim 15 wherein generating the expected values for a next group of digital signals to be stored in the latch responsive to the stored first group of digital signals and storing a second group of digital signals in the latch responsive to the internal clock signal having the first phase are performed at the same time.

20. A method of adaptively adjusting the phase of an internal clock signal relative to an external clock signal, the internal clock signal triggering a latch to store a digital signal, the method comprising:

repetitively applying digital signals to the latch in a known repeating sequence;

storing a first group of digital signals in the latch responsive to the internal clock signal having a first phase;

generating an expect group of digital signals in response to the values of the stored first group of digital signals;

storing a next group of digital signals in the latch responsive to the internal clock signal having the first phase;

comparing the digital signals of the next group to their expected values to determine if the stored digital signals were successfully captured by the latch, and storing the results of this comparison;

adjusting the phase of the internal clock signal;

generating a next expect group of digital signals in response to the values of the current expect group of digital signals;

storing a next group of digital signals in the latch responsive to the internal clock signal having the adjusted phase;

comparing the digital signals of the next group to their expected values to determine if the stored digital signals were successfully captured by the latch, and storing the results of this comparison;

repeating adjusting the phase of the internal clock signal to comparing the digital signals of the next group for a plurality of phases of the internal clock signal; and

selecting a phase of the internal clock signal that caused the latch to store digital signals having the expected values.

21. The method of claim 20 wherein generating a next expect group of digital signals occurs sequentially responsive to the next group of digital signals being stored in the latch.

22. The method of claim 20 wherein repetitively applying digital signals comprises applying a repeating 15 bit pseudo-random bit sequence of digital signals.

23. The method of claim 22 wherein the 15 bit pseudo-random bit sequence comprises the repeating bit sequence of "111101011001000."

24. A pattern generator that generates expect signals for a repeating bit sequence, comprising:

a register having a plurality of inputs and outputs, and a clock terminal adapted to receive a clock signal, the register shifting data applied on each of its inputs to a corresponding output responsive to the clock signals;

a switch circuit having a plurality of first signal terminals adapted to receive respective data input signals, a plurality of second signal terminals coupled to corresponding inputs of the register, and a control terminal adapted to receive a seed signal, the switch circuit coupling each first signal terminal to a corresponding second signal terminal responsive to the seed signal being active; and

a logic circuit coupled between the register inputs and outputs, and having a terminal adapted to receive the seed signal, the logic circuit generating, when the seed signal is inactive, new expect digital signals on the register inputs responsive to current expect digital signals provided on the register outputs.

25. The pattern generator of claim 24 wherein the register comprises a plurality of individual register circuits coupled between each register input and output, each register circuit comprising:

a first pass gate having an input, output, and control terminals adapted to receive respective complementary clock signals;

a first latch having an input coupled to the output of the first pass gate and having an output;

a second pass gate having an input, output, and control terminals adapted to receive the respective complementary clock signals;

a second latch having an input coupled to the output of the second pass gate and having an output; and

a reset switch having signal terminals coupled between the input of the second latch and a supply voltage source, and having a control terminal adapted to receive a reset signal.

26. The pattern generator of claim 24 wherein the switch circuit includes a plurality of pass gates, coupled between respective corresponding first and second signal terminals, and each having complementary control terminals adapted to receive respective true and complement seed signals.

27. The pattern generator of claim 24 wherein the logic circuit includes four outputs, and comprises a plurality of logic gates interconnected to develop as the expect digital signals all possible 4 bit combinations for the 15 bit pseudo-random bit sequence 1111 0101 1001 000, these fifteen possible 4 bit combinations being 1111, 0101, 1001, 0001, 1110, 1011, 0010, 0011, 1101, 0110, 0100, 0111, 1010, 1100, and 1000.

28. The pattern generator of claim 24 wherein the logic circuit comprises:

a combinational logic circuit having a plurality of inputs adapted to receive current expect digital signals from the register outputs and developing a plurality of flip signals responsive to the current expect digital signals; and

a plurality of coupling circuits, each coupling circuit having an input coupled to a corresponding one of the register outputs, an output coupled to the corresponding register input, a first control terminal coupled to the combinational logic circuit, and a second control terminal adapted to receive the seed signal, the coupling circuit operable in a first mode when the seed signal is inactive to develop on its output either the expect data signal applied on its input or the complement of the expect data signal applied on its input responsive to a corresponding one of the flip signals, and operable in a second mode when the seed signal is active to isolate its input from its output.

29. The pattern generator of claim 28 wherein each of the coupling circuits comprises:

an inverter having an input coupled to the corresponding register output, and an output;

an output node coupled to the input of the corresponding register input;

a first switch having a first signal terminal coupled to the output of the inverter, a second signal terminal, and a control terminal adapted to receive the complement of the corresponding one of the flip signals;

a second switch having a first signal terminal coupled to the second signal terminal of the first switch, a second signal terminal coupled to the output node, and a control terminal adapted to receive the seed signal; and

a third switch having a first signal terminal coupled to the register input and a second signal terminal coupled to the second signal terminal of the first switch, and a control terminal adapted to receive the corresponding flip signal.

30. The pattern generator of claim 29 wherein each of the first, second, and third switches is a PMOS transistor, and the coupling circuit further comprises three NMOS transistors coupled in the same way as the three PMOS transistors, each of the NMOS transistors adapted to receive on its gate the complement of the signal applied to the gate of the corresponding one of the PMOS transistors.

31. An integrated circuit having a plurality of external terminals adapted to receive respective signals, comprising:

electronic circuitry having inputs coupled to at least some of the external terminals and outputs coupled to at least some of the external terminals, the electronic circuitry generating signals on its outputs responsive to signals on its inputs to execute a desired function;

a clock terminal adapted to receive an external clock signal;

a clock generator circuit having an input coupled to the clock terminal, and developing an internal clock signal having a phase relative to the external clock signal in response to a phase command;

a latch coupled to at least some of the external terminals and the clock generator circuit, the latch storing digital signals applied on the external terminals responsive to the internal clock signal;

a pattern generator that generates expect data for a repeating bit sequence applied on the external terminals, comprising,

a register having a plurality of inputs and outputs, and a clock terminal adapted to receive a clock signal, the register shifting data applied on each of its inputs to a corresponding output responsive to the clock signals;

a switch circuit having a plurality of first signal terminals coupled to receive latched digital signals from the latch, a plurality of second signal terminals coupled to corresponding inputs of the register, and a control terminal adapted to receive a seed signal, the switch circuit coupling each first signal

terminal to a corresponding second signal terminal responsive to the seed signal being active;

a logic circuit coupled between the register inputs and outputs, and having a terminal adapted to receive the seed signal, the logic circuit generating, when the seed signal is inactive, new expect digital signals on the register inputs responsive to current expect digital signals provided on the register outputs; and

a synchronization circuit coupled to the latch, clock generator, and pattern generator, the synchronization circuit, during a synchronization mode of the integrated circuit, activating the seed signal to seed the pattern generator with a data pattern captured by the latch, and thereafter deactivating the seed signals, sequentially adjusting the phase command, and comparing the digital signals stored by the latch to expected values developed by the pattern generator, the synchronization circuit determining an optimum phase command from the results of the comparisons and applying that phase command to the clock generator during normal operation of the electronic circuitry.

32. The integrated circuit of claim 31 wherein the register comprises a plurality of individual register circuits coupled between each register input and output, each register circuit comprising:

a first pass gate having an input, output, and control terminals adapted to receive respective complementary clock signals;

a first latch having an input coupled to the output of the first pass gate and having an output;

a second pass gate having an input, output, and control terminals adapted to receive the respective complementary clock signals;

a second latch having an input coupled to the output of the second pass gate and having an output; and

a reset switch having signal terminals coupled between the input of the second latch and a supply voltage source, and having a control terminal adapted to receive a reset signal.

33. The integrated circuit of claim 31 wherein the switch circuit includes a plurality of pass gates, each pass gate coupled between a corresponding input and output, and having complementary control terminals adapted to receive respective true and complement seed signals.

34. The integrated circuit of claim 31 wherein the logic circuit includes four outputs, and comprises a plurality of logic gates interconnected to develop as the expect digital signals all possible 4 bit combinations for the 15 bit pseudo-random bit sequence 1111 0101 1001 000, these fifteen possible 4 bit combinations being 1111, 0101, 1001, 0001, 1110, 1011, 0010, 0011, 1101, 0110, 0100, 0111, 1010, 1100, and 1000.

35. The integrated circuit of claim 31 wherein the logic circuit comprises:

a combinational logic circuit having a plurality of inputs adapted to receive current expect digital signals from the register outputs and developing a plurality of flip signals responsive to the current expect digital signals; and

a plurality of coupling circuits, each coupling circuit having an input coupled to a corresponding one of the register outputs, an output coupled to the corresponding register input, a first control terminal coupled to the combinational logic circuit, and a second control terminal adapted to receive the seed signal, the coupling circuit operable in a first mode when the seed signal is inactive to develop on its output either the expect data signal applied on its input or the complement of the expect data signal applied on its input responsive to a corresponding one of the flip signals, and operable in a second mode when the seed signal is active to isolate its input from its output.

36. The integrated circuit of claim 35 wherein each of the coupling circuits comprises:

an inverter having an input coupled to the corresponding register output, and an output;

an output node coupled to the input of the corresponding register input;

a first switch having a first signal terminal coupled to the output of the inverter, a second signal terminal, and a control terminal adapted to receive the complement of the corresponding one of the flip signals;

a second switch having a first signal terminal coupled to the second signal terminal of the first switch, a second signal terminal coupled to the output node, and a control terminal adapted to receive the seed signal; and

a third switch having a first signal terminal coupled to the register input and a second signal terminal coupled to the second signal terminal of the first switch, and a control terminal adapted to receive the corresponding flip signal.

37. The integrated circuit of claim 36 wherein each of the first, second, and third switches is a PMOS transistor, and the coupling circuit further comprises three NMOS transistors coupled in the same way as the three PMOS transistors, each of the NMOS transistors adapted to receive on its gate the complement of the signal applied to the gate of the corresponding one of the PMOS transistors.

38. A packetized dynamic random access memory, comprising:

a clock generator circuit controlling the phase of an internal clock signal relative to an external clock signal responsive to a phase command signal;

at least one array of memory cells adapted to store data at a location determined by a row address and a column address;

a row address circuit adapted to receive and decode the row address, and select a row of memory cells corresponding to the row address responsive to a first set of command signals;

a column address circuit adapted to receive or apply data to one of the memory cells in the selected row corresponding to the column address responsive to a second set of command signals;

a data path circuit adapted to couple data between an external terminal and the column address circuit responsive to a third set of command signals;

a command buffer receiving command packets and initialization packets having a predetermined value, the command buffer including a latch storing each of the received packets responsive to a transition of the internal clock signal, the command buffer further generating a respective command words and initialization words corresponding to each received command packet and initialization packet, respectively;

a pattern generator that generates expect data for a repeating bit sequence applied on external terminals of the packetized dynamic random access memory, comprising,

a register having a plurality of inputs and outputs, and a clock terminal adapted to receive a clock signal, the register shifting data applied on each of its inputs to a corresponding output responsive to the clock signals,

a switch circuit having a plurality of first signal terminals coupled to receive latched digital signals from the latch, a plurality of second signal terminals coupled to corresponding inputs of the register, and a control terminal adapted to receive a seed signal, the switch circuit coupling each first signal terminal to a corresponding second signal terminal responsive to the seed signal being active,

a logic circuit coupled between the register inputs and outputs, and having a terminal adapted to receive the seed signal, the logic circuit generating, when the seed signal is inactive, new expect digital signals on the register inputs responsive to current expect digital signals provided on the register outputs; and

a synchronization circuit coupled to the latch in the command buffer, clock generator, and pattern generator, the synchronization circuit, during a

synchronization mode of the packetized dynamic random access memory, activating the seed signal to seed the pattern generator with a data pattern captured by the latch, and thereafter deactivating the seed signals, sequentially adjusting the phase command, and comparing the digital signals stored by the latch to expected values developed by the pattern generator, the synchronization circuit determining an optimum phase command from the results of the comparisons and applying that phase command to the clock generator during normal operation of the packetized memory device.

39. The packetized dynamic random access memory of claim 38 wherein the register comprises a plurality of individual register circuits coupled between each register input and output, each register circuit comprising:

a first pass gate having an input, output, and control terminals adapted to receive respective complementary clock signals;

a first latch having an input coupled to the output of the first pass gate and having an output;

a second pass gate having an input, output, and control terminals adapted to receive the respective complementary clock signals;

a second latch having an input coupled to the output of the second pass gate and having an output; and

a reset switch having signal terminals coupled between the input of the second latch and a supply voltage source, and having a control terminal adapted to receive a reset signal.

40. The packetized dynamic random access memory of claim 38 wherein the switch circuit includes a plurality of pass gates, each pass gate coupled between a corresponding input and output, and having complementary control terminals adapted to receive respective true and complement seed signals.

41. The packetized dynamic random access memory of claim 39 wherein the logic circuit includes four outputs, and comprises a plurality of logic gates interconnected to develop as the expect digital signals all possible 4 bit combinations for the 15 bit pseudo-random bit sequence 1111 0101 1001 000, these fifteen possible 4 bit combinations being 1111, 0101, 1001, 0001, 1110, 1011, 0010, 0011, 1101, 0110, 0100, 0111, 1010, 1100, and 1000.

42. The packetized dynamic random access memory of claim 38 wherein the logic circuit comprises:

a combinational logic circuit having a plurality of inputs adapted to receive current expect digital signals from the register outputs and developing a plurality of flip signals responsive to the current expect digital signals; and

a plurality of coupling circuits, each coupling circuit having an input coupled to a corresponding one of the register outputs, an output coupled to the corresponding register input, a first control terminal coupled to the combinational logic circuit, and a second control terminal adapted to receive the seed signal, the coupling circuit operable in a first mode when the seed signal is inactive to develop on its output either the expect data signal applied on its input or the complement of the expect data signal applied on its input responsive to a corresponding one of the flip signals, and operable in a second mode when the seed signal is active to isolate its input from its output.

43. The packetized dynamic random access memory of claim 42 wherein each of the coupling circuits comprises:

an inverter having an input coupled to the corresponding register output, and an output;

an output node coupled to the input of the corresponding register input;

a first switch having a first signal terminal coupled to the output of the inverter, a second signal terminal, and a control terminal adapted to receive the complement of the corresponding one of the flip signals;

a second switch having a first signal terminal coupled to the second signal terminal of the first switch, a second signal terminal coupled to the output node, and a control terminal adapted to receive the seed signal; and

a third switch having a first signal terminal coupled to the register input and a second signal terminal coupled to the second signal terminal of the first switch, and a control terminal adapted to receive the corresponding flip signal.

44. The packetized dynamic random access memory of claim 43 wherein each of the first, second, and third switches is a PMOS transistor, and the coupling circuit further comprises three NMOS transistors coupled in the same way as the three PMOS transistors, each of the NMOS transistors adapted to receive on its gate the complement of the signal applied to the gate of the corresponding one of the PMOS transistors.

45. A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a dynamic random access memory coupled to the processor bus adapted to allow data to be stored, adapted to receive a plurality of input signals and generate a plurality of output signals on respective, externally accessible terminals, the dynamic random access memory, comprising,

a clock generator circuit controlling the phase of an internal clock signal relative to an external clock signal responsive to a phase command signal;

at least one array of memory cells adapted to store data at a location determined by a row address and a column address;

a row address circuit adapted to receive and decode the row address, and select a row of memory cells corresponding to the row address responsive to a first set of command signals;

a column address circuit adapted to receive or apply data to one of the memory cells in the selected row corresponding to the column address responsive to a second set of command signals;

a data path circuit adapted to couple data between an external terminal and the column address circuit responsive to a third set of command signals;

a command buffer receiving command packets and initialization packets having a predetermined value, the command buffer including a latch storing each of the received packets responsive to a transition of the internal clock signal, the command buffer further generating a respective command words and initialization words corresponding to each received command packet and initialization packet, respectively;

a pattern generator that generates expect data for a repeating bit sequence applied on external terminals of the packetized dynamic random access memory, comprising,

a register having a plurality of inputs and outputs, and a clock terminal adapted to receive a clock signal, the register shifting data applied on each of its inputs to a corresponding output responsive to the clock signals,

a switch circuit having a plurality of first signal terminals coupled to receive latched digital signals from the latch, a plurality of second signal terminals coupled to corresponding inputs of the register, and a control terminal adapted to receive a seed signal, the switch circuit coupling each first signal terminal to a corresponding second signal terminal responsive to the seed signal being active,

a logic circuit coupled between the register inputs and outputs, and having a terminal adapted to receive the seed signal, the logic circuit generating, when the seed signal is inactive, new expect digital signals on the register inputs responsive to current expect digital signals provided on the register outputs; and

a synchronization circuit coupled to the latch in the command buffer, clock generator, and pattern generator, the synchronization circuit, during a synchronization mode of the packetized dynamic random access memory, activating the seed signal to seed the pattern generator with a data pattern captured by the latch, and thereafter deactivating the seed signals, sequentially adjusting the phase command, and comparing the digital signals stored by the latch to expected values developed by the pattern generator, the synchronization circuit determining an optimum phase command from the results of the comparisons and applying that phase command to the clock generator during normal operation of the packetized memory device.

46. The computer system of claim 45 wherein the register comprises a plurality of individual register circuits coupled between each register input and output, each register circuit comprising:

a first pass gate having an input, output, and control terminals adapted to receive respective complementary clock signals;

a first latch having an input coupled to the output of the first pass gate and having an output;

a second pass gate having an input, output, and control terminals adapted to receive the respective complementary clock signals;

a second latch having an input coupled to the output of the second pass gate and having an output; and

a reset switch having signal terminals coupled between the input of the second latch and a supply voltage source, and having a control terminal adapted to receive a reset signal.

47. The computer system of claim 45 wherein the switch circuit includes a plurality of pass gates, each pass gate coupled between a corresponding input and output, and having complementary control terminals adapted to receive respective true and complement seed signals.

48. The computer system of claim 46 wherein the logic circuit includes four outputs, and comprises a plurality of logic gates interconnected to develop as the expect digital signals all possible 4 bit combinations for the 15 bit pseudo-random bit sequence 1111 0101 1001 000, these fifteen possible 4 bit combinations being 1111, 0101, 1001, 0001, 1110, 1011, 0010, 0011, 1101, 0110, 0100, 0111, 1010, 1100, and 1000.

49. The computer system of claim 45 wherein the logic circuit comprises:

a combinational logic circuit having a plurality of inputs adapted to receive current expect digital signals from the register outputs and developing a plurality of flip signals responsive to the current expect digital signals; and

a plurality of coupling circuits, each coupling circuit having an input coupled to a corresponding one of the register outputs, an output coupled to the corresponding register input, a first control terminal coupled to the combinational logic circuit, and a second control terminal adapted to receive the seed signal, the coupling circuit operable in a first mode when the seed signal is inactive to develop on its output either the expect data signal applied on its input or the complement of the expect data signal applied on its input responsive to a corresponding one of the flip signals, and operable in a second mode when the seed signal is active to isolate its input from its output.

50. The computer system of claim 49 wherein each of the coupling circuits comprises:

an inverter having an input coupled to the corresponding register output, and an output;

an output node coupled to the input of the corresponding register input;

a first switch having a first signal terminal coupled to the output of the inverter, a second signal terminal, and a control terminal adapted to receive the complement of the corresponding one of the flip signals;

a second switch having a first signal terminal coupled to the second signal terminal of the first switch, a second signal terminal coupled to the output node, and a control terminal adapted to receive the seed signal; and

a third switch having a first signal terminal coupled to the register input and a second signal terminal coupled to the second signal terminal of the first switch, and a control terminal adapted to receive the corresponding flip signal.

51. The computer system of claim 50 wherein each of the first, second, and third switches is a PMOS transistor, and the coupling circuit further comprises three NMOS transistors coupled in the same way as the three PMOS transistors, each of the NMOS transistors adapted to receive on its gate the complement of the signal applied to the gate of the corresponding one of the PMOS transistors.